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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,680	10/13/2000	Ville Eerola	PM 274422/2990978US	7630

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CROWELL & MORING LLP
INTELLECTUAL PROPERTY GROUP
P.O. BOX 14300
WASHINGTON, DC 20044-4300

EXAMINER	
BAYARD, EMMANUEL	

ART UNIT	PAPER NUMBER
2638	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/689,680	EEROLA ET AL.	
	Examiner	Art Unit	
	Emmanuel Bayard	2638	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is in response to RCE filed on 5/16/05 in which claims 1-22 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3 and 9-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatani U.S. Patent No 6,496,474 in view of Ozluturk et al US Pub No 20050094604 A1.

As per claim 1, Nagatani et al discloses a device for generating a t least one code phase, comprising: a shift register comprising N outputs (see figs.2, 6, -15, 18 elements 3, 41, 72 and col.4, lines 5-17) and input to which a data generator is the same as the claimed (code sequence) (see element 1 and col.4, lines 4-17) to be phased is applied, N being an integer greater than two; a M sequence generator is considered as the claimed (at least one logic branch) (see figs. 2, 6-15, 16 elements 3, 42, 51, 61 and col.4, lines 7-67 and col.5, lines 1-5 and col.6, lines 33-50), controlled by at least a clock generator is the same as the claimed (one combination control signal) (see fig.2 element 4 and col.4, lines 11-14), on the basis of which the logic branch adds is considered as the claimed (combines) (see figs. 2, 3a elements 12-13 and col.4, lines

37-50 and col.5, lines 1-18) the code phase from I outputs of the shift register, I being an integer between 2 and N.

However Nagatani does not teach wherein said combination control signal is usable to set one or more weighting coefficients.

Ozluturk et al teaches wherein said combination control signal is usable to set one or more weighting coefficients (see fig. 8b element W1-WI and page 21, paragraph [0253].

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ozluturk et al into Nagatani as to correct the channel response of each multipath signal so that the maximum detection value could be generated as taught by Ozluturk (see page 21 paragraph [0256]).

As per claim 2, the device of Nagatani does include (I two-input selectors) (see fig.7, 11-13 elements SW52 and col.7, lines 10-35), to the first input of each of which is connected one input of the shift register and to the second input is connected one combination control signal and adders is considered as the claimed (I-input combiner) (see fig.7), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

As per claim 3, the device of Nagatani does include a first logic branch comprising M1 two-input selectors (see fig.7, 11-13) to which the outputs of M1 registers of the shift register and M1 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and

one combination control signal, and M1-input combiner (see fig.7, 11-13), to whose inputs are connected the outputs of said M1 selectors and from whose output the first code phase is obtained (see fig.7, 11-13) ; a second logic branch comprising M2 tow-input selectors ((see fig.7, 11-13) to which the outputs of M2 registers of the shift register and M2 combination control signals are connected in such a way that to the inputs of each selector is connected one output of the shift register and one combination control signal, and an M2-input combiner (see fig.7, 11-13) to whose inputs are connected the outputs of said M2 selectors and from whose output the second code phase is obtained (((see fig.7, 11-13).

As per claim 9, the device of Ozluturk teaches a weight software (see paragraphs [0596, 0617]. Furthermore implementing such software into Nagatani would have been obvious to one skilled in the art as to accurately transmit code messages without interruption during the process.

As per claim 10, the device of Ozluturk teaches multipliers and/or AND gates. (see paragraphs [0252, 0567]). Furthermore implementing such teaching into Nagatani would have been obvious to one skilled in the art as to accurately transmit code messages without interruption during the process

As per claim 11, the device of Nagatani does include are adders and/or OR gates (see fig.3a).

As per claim 12, the device of Ozluturk teaches weighting coefficients. Furthermore implementing such teaching into Nagatani would have been obvious to one skilled in the art as to correct the channel response of each multipath signals so that the

maximum detection value could be generated as taught by Ozluturk (see page 21 paragraph [0256]).

As per claims 13 and 16, the device of Nagatani discloses a correlator comprising: generation means comprising a code generator for generating local code (see fig.2 element 10 and col.5, lines 14-15), and a shift register (see figs.2, 6, -15, 18 elements 3, 41, 72 and col.4, lines 5-17), the generation means generating at least one code phase from said local code; at least matched filter is functionally equivalent to the claimed (to at least one correlator) (see fig.17 element 123 col.5, lines 55-57 and col.11, lines 20-25 and col.13, lines 30-31) for correlating a signal applied to the correlator structure with said at least on locally generated code phase, said generation means further comprising a M sequence generator is considered as the claimed (at least one logic branch) (see figs. 2, 6-15, 16 elements 3, 42, 51, 61 and col.4, lines 7-67 and col.5, lines 1-5 and col.6, lines 33-50), controlled by at least a clock generator is the same as the claimed (one combination control signal) (see fig.2 element 4 and col.4, lines 11-14), on the basis of which the logic branch adds is considered as the claimed (combines) (see fig.3a) the code phase from I outputs of the shift register, I being an integer between 2 and N.

However Nagatani does not teach wherein said combination control signal is usable to set one or more weighting coefficients.

Ozluturk et al teaches wherein said combination control signal is usable to set one or more weighting coefficients (see fig. 8b element W1-WI and page 21, paragraph [0253].

It would have been obvious to one of ordinary skill in the art to implement the teaching of Ozluturk et al into Nagatani as to correct the channel response of each multipath signal so that the maximum detection value could be generated as taught by Ozluturk (see page 21 paragraph [0256]).

As per claims 14 and 17, the correlator of Nagatani does include (I two-input selectors) (see fig.7, 11-13 elements SW52 and col.7, lines 10-35), to the first input of each of which is connected one input of the shift register and to the second input is connected to one combination control signal and adders is considered as the claimed (I-input combiner) (see fig.7), to whose outputs are connected the outputs of said I selectors and from whose output said code phase is obtained.

As per claims 15 and 18, the device of Ozluturk teaches weight software (see paragraphs [0596, 0617]. Furthermore implementing such software into Nagatani would have been obvious to one skilled in the art as to accurately transmit code messages without interruption during the process.

As per claim 19 the device of Ozluturk teaches spreading code (see paragraph [0017]. Furthermore implementing such code as replica into Nagatani would have been obvious to one skilled in the art as to accurately transmit code messages without interruption during the process.

As per claims 20-22, the device of Ozluturk teaches one or more weighting coefficients (see fig. 8b element W1-WI and page 21, paragraph [0253]. Furthermore

implementing such teaching into Nagatani would have been obvious to one skilled in as to correct the channel response of each multipath signals so that the maximum detection value could be generated as taught by Ozluturk (see page 21 paragraph [0256]).

Claim Rejections - 35 USC э 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagatani U.S. Patent No 6,496,474 B1 in view of Ozluturk et al US Pub No 20050094604 A1 and in further view of Nakamura et al U.S. Patent NO 6,275,520 B.

1. As per claims 4-6, Nagatani and Ozluturk in combination teaches all the features of the claimed invention except a third logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a third branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Nagatani and Ozluturk as to provide desired shift amounts

and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

As per claims 7-8, Nagatani and Ozluturk teaches all the features of the claimed invention except a fourth logic branch connected directly to the output of one register of the shift register and from which the third code phase is obtained.

Nakamura et al teaches a fourth branch (see figs.2, 9 element 16) connected directly to the output of one register of the shift registers (see fig.2 element 10) and from which the third code phase is obtained (see col.1, lines 36-45 and col.2, lines 60-65).

It would have been obvious to one of ordinary skill in the art to incorporate the teaching of Nakamura into Nagatani and Ozluturk as to provide desired shift amounts and each pattern would be prestored in the storage location in the ROM as taught by Nakamura (see col.2, lines 63-65).

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mcrae et al U.S. Patent No 4,365,338 teaches a technique for high rate digital transmission.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (7:Am-4:30PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vanderpuye Kenneth can be reached on 571 272 3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2638

7/7/05

EMMANUEL BAYARD
PRIMARY EXAMINER